

FORM PTO-1449 U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTY. DOCKET NO. ARC.003A	APPLICATION NO. 09/801,241
INFORMATION DISCLOSURE STATEMENT BY APPLICANT		APPLICANT David Latta	JAN 16 2002 Technology Center 2100 RECEIVED
JAN 09 2002 (USE SEVERAL SHEETS IF NECESSARY)		FILING DATE March 7, 2001	

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (IF APPROPRIATE)
AKm	5,247,637	09/21/93	Leedom, et al.			
1	5,394,515	02/28/95	Lentz, et al.			
2	5,481,707	01/02/98	Murphy, et al.			
3	5,537,604	07/16/96	Baum, et al.			
4	5,558,851	09/24/96	Lentz, et al.			
5	5,584,117	10/06/96	Lentz, et al.			
6	5,636,364	06/03/97	Emma, et al.			
7	5,960,468	09/28/98	Edward J. Paluch			
8	5,968,114	10/19/98	Wentka, et al.			
9	5,987,574	11/16/98	Edward J. Paluch			
10	6,038,646	03/14/00	Robert F. Sproul			
11	6,091,431	07/18/00	Saxena, et al.			
12	6,092,167	07/18/00	Cheung, et al.			
13	6,141,739	10/31/00	Provence, et al.			
14	6,182,192	01/30/01	Fabrizio Rovati			
15	6,240,492	05/29/01	Foster, et al.			
16						
17						

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
						YES	NO

EXAMINER INITIAL	OTHER DOCUMENTS (INCLUDING AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.)	
AKm	17	Application Serial No. 09/418,663 entitled "Method and Apparatus for Managing the Configuration and Functionality of a Semiconductor Design," filed October 14, 1999 - Attorney Docket No. ARC.001A

EXAMINER	DATE CONSIDERED
Dornan & Mason	12-8-2003

*EXAMINER: INITIAL IF CITATION CONSIDERED, WHETHER OR NOT CITATION IS IN CONFORMANCE WITH MPEP 609; DRAW LINE THROUGH CITATION IF NOT IN CONFORMANCE AND NOT CONSIDERED. INCLUDE COPY OF THIS FORM WITH NEXT COMMUNICATION TO APPLICANT.

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	APPLICANT David Latta	
	FILING DATE March 7, 2001	GROUP 2181

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EXAMINER INITIAL	OTHER DOCUMENTS (INCLUDING AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.)	
<i>AKM</i>	2	The CoreConnect Bus Architecture - XP-002204519 by International Business Machines Corporation, 1999.
	3	Embedded DRAM for a Reconfigurable Array - XP-000894790 by Symposium on VLSI Circuits Digest of Technical Papers
	4	A Scalable Architecture for System-On-Chip Interconnections - XP-002204520 by Pierre Guerrier and Alain Greiner dated October 22, 1999.
	5	A Reconfigurable Bus IP for Modular Function Integration - XP-002204520 by Neil S. Stollen, Ph.D., P.E. at Infinite Technology Corp. dated March 22, 1999.

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